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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,358	09/15/2000	Taiji Noda	0819-0423	1724

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NIXON PEABODY, LLP
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN, VA 22102

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,358	NODA ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-15 and 21-24* is/are pending in the application.

4a) Of the above claim(s) *1-5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10,12-15 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on June 18, 2003 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,432,802 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Status of the Claims

2. Amendment filed June 18, 2003 has been entered as Paper No. 23. Claim 20 has been canceled. Claims 1-10,12-15 and 21-24 are pending. Claims 1-5 have been withdrawn.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE HAVING A POCKET DOPANT DIFFER THAN DOPANT OF AN EXTENDED HIGH-CONCENTRATION DIFFUSED LAYER.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 6-10, 12-14 and 2133-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over G.G. Shahidi et al., *High-Performance Devices for a 0.15 μm CMOS Technology*, in view of Burr (U.S. Patent No. 5,923,987) all of record.

Shahidi teaches a method for fabricating a semiconductor device that includes an extended high-concentration dopant (As) diffused layer of a first conductivity and a pocket dopant (In) diffused layer of a second conductivity substantially as claimed including:

a first step of forming a gate electrode over a semiconductor region with a gate insulating film interposed therebetween;

a second step of implanting heavy ions (In) into the semiconductor region on both side of the gate electrode using the gate electrode as a mask, thereby forming a first (In) ion implanted layer of the second conductivity type (p), at least upper part of which is an amorphous layer;

a third step of implanting ions (As) of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second (As) ion implanted layer of the first conductivity type (n); and

wherein the pocket dopant (In) diffused layer includes, in a portion in contact with the extended high-concentration dopant (As) diffused layer, a segregated part that has been formed through segregation of the heavy (In) ions. (See page 466-468).

Thus, Shahidi is shown to teach all the features of the claim with the exception of explicitly disclosing an anneal process to activate the first and second implanted dopants.

However, Burr teaches following the implantations of the first (347) and second (336) implanted layers, conducting a first annealing process to activate the first (347) and second (336) ion implanted layers, thereby forming the extended high-concentration dopant diffused layer (336) of the first conductivity type (n) through diffusion of the first dopant and the pocket dopant diffused layer (347) of the second conductivity type (p), which is in contact with bottom portion

of the extended high-concentration dopant diffused layer (336), through diffusion of the heavy ions (347), respectively.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to conduct a first annealing process to activate the first (In) and second (As) implanted dopants of Shahidi as taught by Burr because the process step is well known in the art. (See col. 15, lines 1-9).

With respect to claim 7, the segregated part of the pocket dopant (In) diffused layer of Shahidi appears to overlap with a profile of the extended high-concentration dopant (As) diffused layer. Also see Burr, Fig. 5H.

With respect to claim 8, method of Shahidi in view of Burr further includes:

forming a sidewall spacer on side faces of the gate electrode after the third step has been performed;

implanting ions of a second dopant into the semiconductor region using the gate electrode and the sidewall spacer as a mask, thereby forming a third ion implanted layer of the first conductivity type (n); and

conducting a second annealing process to activate the third ion implanted layer, thereby forming a high-concentration dopant diffused layer of the first conductivity type, which is located outside of the extended high-concentration dopant diffused layer (336A), has a junction deeper than that of the extended high-concentration dopant diffused layer (336A) and has been formed through diffusion of a second dopant.

With respect to claim 9, the heavy ions (In) of Shahidi are implanted at such an implant energy as forming an amorphous crystalline interface, through implantation of the heavy ions (In), at a level equal to or deeper than a range of the first dopant and shallower than a range of the second dopant.

With respect to claim 10, method of Shahidi in view of Burr further includes:

implanting ions into a surface part of the semiconductor region, thereby forming a fourth ion implanted (channel) layer of a second conductivity type (p) before the first step is performed; and

conducting a third annealing process to activate the fourth ion implanted layer, thereby forming a dopant diffused layer (334) to be a channel region. (Also see Fig. 5B).

With respect to claim 12, the heavy ions (In) of Shahidi are implanted at such an implant energy as getting a range of the heavy ions (In) equal to or deeper than a range of the first dopant (As) and between one to three times as deep as the range of the first dopant (As).

With respect to claim 13, the heavy ions of Shahidi and Burr includes indium ions.

With respect to claim 14, the implant dose of the heavy ions of Shahidi in view of Burr is within the order of magnitude as claimed.

Further, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum dose of the ions implanted. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

With respect to claim 21, the first dopant of Shahidi and Burr is arsenic.

With respect to claim 22, the heavy ions of Shahidi and Burr are indium ions.

With respect to claim 23, the heavy ions and the first dopant of Shahidi are indium ions and arsenic and the second dopant, in view of Burr '987, are arsenic.

With respect to claim 24, the fourth ion implanted layer of Shahidi id formed into the surface part of the semiconductor region by implanting indiums ions.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shahidi et al. and Burr '987 as applied to claim 6 above, and further in view of Tsukamoto (U.S. Patent No. 5,399,506) (cited previously).

Shahidi and Burr '987 teach conducting the first annealing process using a rapid thermal annealing (RTA) as is well known to those skill in the art.

Thus, Shahidi and Burr '987 are shown to teach all the features of the claim with the exception of explicitly disclosing the details of RTA process.

However, Tsukamoto teaches that RTA process is well known in the art including: a semiconductor region is heated up to a temperature between 950 °C and 1050 °C at a rate between 100 °C/sec to 150 °C/sec and then kept at the temperature for a period of time between 1 to 10 seconds.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention perform the RTA process of Shahidi and Burr as taught by Tsukamoto to activate the dopants.

Further, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum annealing temperature and the temperature rate of increase to activate the dopant. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

Response to Arguments

6. Applicant's arguments filed June 18, 2003 have been fully considered but they are not persuasive.

With respect to claim 6, Applicants appears to contend, by way of Fig. B (attachment), that the heavy ions (In) and the extended high-concentration dopant diffused layer are not segregated.

However, Applicant is urged to pay attention to col. 2 of page 466, Shahidi et al., "the In (heavy ions, pocket dopant) and Sb channel implant peaks were placed at about 100 nm under the channel.....The nFET extension is about 50 nm deep and pFET extension is about 60 nm deep". Clearly they are segregated.

Claim 6 and the dependent claims thereof are obvious over the combination of the references. The rejections are therefore, maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LONG PHAM
PRIMARY EXAMINER

A.M
September 2, 2003